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APPLICATION NUMBER	FILING DATE	FIRST NAMED APPLICANT	ATTORNEY DOCKET NO.
08/707,694	09/04/96	RANGASAYEE K	64.663-063

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TM01/1213

EXAMINER	
BUTLER, D	
ART UNIT	**PAPER NUMBER**
2182	16

DATE MAILED: 12/13/00

This is a communication from the examiner in charge of your application.
COMMISSIONER OF PATENTS AND TRADEMARKS

OFFICE ACTION SUMMARY

☒ Responsive to communication(s) filed on 10-2-00.

☒ This action is **FINAL**.

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle*, 1935 D.C. 11; 453 O.G. 213.

A shortened statutory period for response to this action is set to expire three month(s), or thirty days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133). Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

Disposition of Claims

☒ Claim(s) 2-10, 12 and 15-24 is/are pending in the application.

Of the above, claim(s) _____ is/are withdrawn from consideration.

☐ Claim(s) _____ is/are allowed.

☒ Claim(s) 2-10, 12 and 15-24 is/are rejected.

☐ Claim(s) _____ is/are objected to.

☐ Claims _____ are subject to restriction or election requirement.

Application Papers

☐ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

☐ The proposed drawing correction, filed on _____ is ☐ approved ☐ disapproved.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☐ All ☐ Some* ☐ None of the CERTIFIED copies of the priority documents have been

☐ received.

☐ received in Application No. (Series Code/Serial Number) _____.

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____.

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

☒ Notice of Reference Cited, PTO-892

☐ Information Disclosure Statement(s), PTO-1449, Paper No(s). _____

☐ Interview Summary, PTO-413

☐ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Notice of Informal Patent Application, PTO-152

-- SEE OFFICE ACTION ON THE FOLLOWING PAGES --

* U.S. GPO: 1996-409-290/40029

1. This action is in response to paper number 15, Amendment C, which was received on October 2, 2000. Claims 2-10, 12 and 15-24 are pending.

2. The text of those sections of Title 35, US Code not included in this action can be found in a prior Office Action.

3. Claims 3-4 are rejected under 35 USC § 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

The specification as filed does not properly describe that a programmable logic circuit "comprises a product term array" and "comprises a look-up table". The examiner could find no description in the specification that would enable on of ordinary skill in the art to make and/or use the claimed elements without undue experimentation.

In the remarks applicant argued that a person of ordinary skill in the art of programmable logic devices would know that the logic blocks of FIG. 3 could contain a look-up table or a product term array. The examiner disagrees with applicant's contentions. The claim language recites a programmable logic circuit and is not limited to the programmable logic device having the logic blocks of FIG. 3. Applicant has failed to provide any evidence that a person of ordinary skill in the art would know that a programmable logic circuit configured to generate one or more control signals and receive one or more clock signals would comprise a product term array or a look-up

table. Applicant seems to be using hindsight in order to add new matter to the specification. In addition, applicant has failed to provide any motivation or suggestion why one of ordinary skill in the art would add a product term array or a look-up table to a programmable logic circuit configured to generate one or more control signals and receive one or more clock signals. The specification at the time of filing provided no description of a programmable logic circuit configured to generate one or more control signals and receive one or more clock signals which comprised a product term array or a look-up table.

4. Claims 2, 6, 10, 12, 15-16, 18 and 20-23 are rejected under 35 USC 102(e) as being anticipated by Chou et al., U.S. Patent 5,710,524.

Per claim 12:

A) Chou et al teach the following claimed items:

1. a programmable logic circuit with PLA 8, counter 6 and counter 9 of figure 5 and at column 4, lines 8-34;
2. a phase lock loop circuit with the interconnection of elements 2, 3 and 4 of figure 5, at column 4, lines 8-15, at column 1, lines 5-13 and with the Abstract.

Per claims 15 and 22:

A) Chou et al teach the following claimed items:

1. means for implementing/manipulating information to generate to generate a control signal and receive a clock with PLA 8, counter 6 and counter 9 of figure 5 and at column 4, lines 8-34;
2. means for generating a clock signal with the interconnection

of elements 2, 3 and 4 of figure 5, at column 4, lines 8-15, at column 1, lines 5-13 and with the Abstract.

Per claims 2, 6, 16 and 23:

Chou teaches providing a clock signal which is individually programmable to a plurality of frequencies with Fosc of figure 5 and with the Abstract.

Per claim 10:

Chou teaches a device consisting of a programmable logic array 8 of figure 5.

Per claims 18 and 20:

Chou teaches selecting a reference clock frequency from an internal clock signal with PLA 8 and Counter 6 of figure 5 and at column 4, lines 24-67 and with the Abstract.

Per claim 21:

Chou teaches the programmable logic circuit generating an output signal (the outputs of PLA8 or Counter 6 or Counter 9) in response to an input signal (SEL0 or SEL1) and a clock signal (reference clock) with figure 5.

5. Claims 7-9 and 19 are rejected under 35 USC 103 as being unpatentable over Chou et al., U.S. Patent 5,710,524, in view of Davis et al., U.S. Patent 4,893,271.

Per claims 7-9 and 19:

Chou et al teach the reference clock comprising one or more clock frequencies with the reference clock output from Programmable Counter 6 of figure 5 and with the Abstract. Chou teaches that it is known to select from one or more reference frequencies with Programmable counter 6 of figure

5 which is functionally equivalent to selecting from one or more reference frequencies using a multiplexer. Davis et al teach the reference clock comprising one or more clock frequencies with the reference clock output on line 202 of figures 2, 3 and 4. Davis teaches that it is known to select from one or more reference frequencies with Variable Divider 106 of figure 1b which is functionally equivalent to selecting from one or more reference frequencies using a multiplexer. In addition, Davis teaches that it is well known to include a multiplexer in an integrated circuit for selecting one of a plurality of clock frequencies in response to a configuration signal with Timing Selector 218 of figure 3 and Timing Selector 206 of figure 4 and at column 11, lines 53-58. Davis describes that it is well known to generate external reference clock signals with figures 1B, 3 and 4. Chou teaches generating a reference clock frequency from an internal clock signal with PLA 8 and Counter 6 of figure 5 and at column 4, lines 24-67 and with the Abstract. In addition, claim 20 is evidence that generation of the reference clock internally or externally is a matter of design choice. One of ordinary skill in the art would have been motivated to combine Davis and Chou because of Davis's suggestion at column 1, lines 16-46. It would have been obvious for one of ordinary skill in the art to combine Davis and Chou because they are both directed to the problem of generating a plurality of phase locked clock signals for a programmable logic device.

6. Claims 5, 17 and 24 are rejected under 35 USC 103 as being unpatentable over Chou et al., U.S. Patent 5,710,524, in view of Appel, U.S. Patent 5,544,047.

Per claims 5, 17 and 24:

Regarding Claims 5, 17 and 24, the recited functions are well known in the timing and integrated circuit design art as described by Appel at column 5, lines 36-52, at column 7, line 59 - column 8, line 6 and at column 10, lines 44-61 and would have been obvious to one of ordinary skill in the art. One of ordinary skill in the art would have been motivated to combine Chou and Appel because of Appel's suggestion at column 1, lines 7-12 and at column 10, lines 44-61.

7. Claims 22-23 are rejected under 35 USC 102(e) as being anticipated by Weiss et al., U.S. Patent 5,774,703.

Per claims 22-23:

A) Weiss et al teach the following claimed items:

1. means for implementing programmable logic for manipulating information to generate control signals with Registers 200, 250 and 300 of figure 1 and at column 2, line 36 - column 3, line 4;

2. means for generating a clock signal in response to a reference clock frequency each capable of oscillating at a different one of a plurality of frequencies with figures 4 and 5 and at column 5, line 47 - column 8, line 21.

8. In the remarks, applicants argued in substance that:

A) The Office Action mischaracterizes the disclosure of Chou et

al. The PLA 8 only has inputs SEL0 and SEL1 which are used to select dividing numbers. PLA 8 receives no clock signals as inputs.

B) The clock signals of Weiss et al. are not generated in response to a reference clock and one or more control signals.

C) Weiss et al. does not disclose or suggest the means for implementing programmable logic and the means for generating.

9. As to point A, the examiner disagrees with applicant's contentions. Applicant has mischaracterized the Office Action. The Office Action present in applicant's file, paper number 14, paragraph 7, clearly indicates that the examiner pointed to PLA 8, counter 6 and counter 9 of figure 5 as the claimed programmable logic **circuit**. The examiner did not rely solely on PLA 8 as the programmable logic circuit. The circuit of PLA 8, counter 6 and counter 9 teach the claimed elements as described in the art rejection including receiving one or more clock signals. The Microsoft Press Computer Dictionary recites that a circuit is any path that can carry electrical current. More generally, the term is used to refer to a combination of electrical components interconnected to perform a particular task. At one level, a computer consists of a single circuit; at another, it consists of hundreds of interconnected circuits. Therefore, Chou et al teach the claimed invention.

As to point B, Weiss teaches a reference clock with clock Fo of figure 4 as described in the art rejection. Weiss clearly teaches generating control signals with Registers 200, 250 and 300 of figure 1 and at column 2, line 36 - column 3, line 4.

As to point C, the examiner disagrees with applicant's contentions. Weiss clearly teaches all the claimed elements as described in the above art rejection.

10. **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR § 1.136(a).

A SHORTENED STATUTORY PERIOD FOR RESPONSE TO THIS FINAL ACTION IS SET TO EXPIRE THREE MONTHS FROM THE DATE OF THIS ACTION. IN THE EVENT A FIRST RESPONSE IS FILED WITHIN TWO MONTHS OF THE MAILING DATE OF THIS FINAL ACTION AND THE ADVISORY ACTION IS NOT MAILED UNTIL AFTER THE END OF THE THREE-MONTH SHORTENED STATUTORY PERIOD, THEN THE SHORTENED STATUTORY PERIOD WILL EXPIRE ON THE DATE THE ADVISORY ACTION IS MAILED, AND ANY EXTENSION FEE PURSUANT TO 37 CFR § 1.136(a) WILL BE CALCULATED FROM THE MAILING DATE OF THE ADVISORY ACTION. IN NO EVENT WILL THE STATUTORY PERIOD FOR RESPONSE EXPIRE LATER THAN SIX MONTHS FROM THE DATE OF THIS FINAL ACTION.

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dennis M. Butler whose telephone number is (703) 305-9663. The examiner can normally be reached on Monday-Friday from 9:30 AM to 6:00 PM.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 305-3900.

Dennis M. Butler
December 11, 2000

Dennis M. Butler
Primary Examiner
Group 2180